NON-VOLATILE MEMORY AND METHOD WITH IMPROVED SENSING

ABSTRACT OF THE DISCLOSURE

Source line bias is an error introduced by a non-zero resistance in the ground loop of the read/write circuits. During sensing the control gate voltage of a memory cell is erroneously biased by a voltage drop across the resistance. This error is minimized when the current flowing though the ground loop is reduced. A method for reducing source line bias is accomplished by read/write circuits with features and techniques for multi-pass sensing. When a page of memory cells are being sensed in parallel, each pass helps to identify and shut down the memory cells with conduction current higher than a given demarcation current value. In particular, the identified memory cells are shut down after all sensing in the current pass have been completed. In this way the shutting down operation does not disturb the sensing operation. Sensing in subsequent passes will be less affected by source line bias since the total amount of current flow is significantly reduced by eliminating contributions from the higher current cells. In another aspect of sensing improvement, a reference sense amplifier is employed to control multiple sense amplifiers to reduce their dependence on power supply and environmental variations.